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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/320,833	05/26/99	SINGH B	99P7613US

TM02/0524

SIEMENS CORPORATION
INTELLECTUAL PROPERTY DEPARTMENT
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EXAMINER	
PATEL, G	
ART UNIT	**PAPER NUMBER**
2183	2

DATE MAILED: 05/24/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

PTO-90C (Rev.11/00)

1- File Copy

Office Action Summary

Application No.	Applicant(s)
09/320,833	Singh et al.
Examiner	**Art Unit**
Gautam R. Patel	2183

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *three* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☐ Responsive to communication(s) filed on _____

2a) ☐ This action is **FINAL.** 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-13* is/are pending in the applica

4a) Of the above, claim(s) _____ is/are withdrawn from considera

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-13* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirem

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)

16) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)

17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____

18) ☐ Interview Summary (PTO-413) Paper No(s). _____

19) ☐ Notice of Informal Patent Application (PTO-152)

20) ☐ Other:

DETAILED ACTION

1. Claims 1-13 are pending for the examination.

Specification

2. The disclosure is objected for following reasons.

The title of the invention is neither precise nor descriptive. A new title is required which should include, using twenty words or fewer, claimed features that differentiate the invention from the Prior Art. The title should reflect the gist of or the improvement of the present invention.

Correction is required.

Claim Objections

3. Claims 1-13 are objected for following reasons.

Claim 1, line 5, states "the validity and size of said prefetch buffer" is confusing in the light of the fact that specification clearly indicates that validity and size of the data in the prefetch buffer is indicated. This language creates confusion that size of prefetch buffer is in question and not the data.

Similarly claim 3, lines 5-6 and claim 9 lines 6-7 also states "the validity and size of said prefetch buffer", which is confusing for the same reasons stated above.
NOTE: For examination purposes it is assumed that the Applicants are claiming the size and validity of the data and not the prefetch buffer itself.

Corrections are required.

Drawings

4. The drawings are objected for following reasons:

a. The drawings are objected to under 37 C.F.R. § 1.83(a). The drawings must show *every feature* of the invention specified in the claims. Therefore, the steps shown in claims 1-13 must be shown or the feature cancelled from the claim. No new matter should be entered.

b. The structural elements are merely labeled with identifying numbers, see Figs. 3-4 and 5. Since these elements are not illustrated as well known graphical representations, Applicant is required to provide suitable meaningful legends under 37 CFR § 1.83 (a) and 1.84 (o).

Correction are required.

Applicant is required to submit a proposed drawing correction in response to this Office Action. Any proposal by the applicant for amendment of the drawings to cure defects must consist of two parts:

c. A separate letter to the Draftsman in accordance with MPEP § 608.02 (r); and,

d. A print or pen-and-ink sketch showing changes in ***red ink*** in accordance with MPEP § 608.02 (v).

IMPORTANT NOTE: The filing of new formal drawings to correct the noted defect may be deferred until the application is allowed by the examiner, but the print or pen-and-ink sketch with proposed corrections shown in *red ink* is required in response to this Office Action, and may not be deferred.

Claim Rejections - 35 U.S.C. § 103

5. The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Subject matter developed by another person, which qualifies as prior art only under subsection (f) or (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. § 103, the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 C.F.R. § 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of potential 35 U.S.C. § 102(f) or (g) prior art under 35 U.S.C. § 103.

6. Claims 1-8 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Divivier et al., US. patent 5,689,564 (hereafter Divivier) in view of Adler et al., US. patent 4,811,284 (hereafter Adler).

As to claim 1, Divivier discloses the invention as claimed [see Figs. 1-3] including steps of requesting data, setting data for validity in a prefetch buffer under condition of valid and invalid data comprising the steps of:

Method for providing a plurality of aligned instructions from an instruction stream provided by a memory unit for execution within a pipelined microprocessor [fig. 1; col. 3, lines 14-25] comprising a prefetch buffer [fig. 1, unit 12], whereby said prefetch buffer stores prefetched instructions and additional information about the validity [fig. 3, units pf0 and pf1] of data in said prefetch buffer, said method comprising the steps of:

- in case said prefetch buffer containing invalid data [col. 8, lines 15-16]:

a) requesting an instruction stream and storing said instruction stream in said prefetch buffer [col. 7, lines 36-44]; [note: zero indicates invalid data, and invalid data is found valid data is requested from external memory and stored in the prefetch buffer]

b) setting said data for validity in said prefetch buffer [col. 7, line 59 to col. 8, line 16];

c) issuing a requested number of instructions from said requested instruction stream [col. 7, line 59 to col. 8, line 16]; and

e) invalidating said validity data if all instructions from said prefetch buffer have been issued [col. 9, lines 24-35]; [NOTE: when buffer is empty all data positions are empty and now valid bits are set to "0" i.e. making them invalid for new data to come in]; also

- in case said prefetch buffer contains valid data [col. 8, lines 15-16]:

f) issuing a requested number of instructions from said prefetch buffer [col. 7, line 59 to col. 8, line 16]; and

h) invalidating said validity data if all instructions from said prefetch buffer have been issued [col. 9, lines 24-35]; [NOTE: when buffer is empty all data positions are empty and now valid bits are set to "0" i.e. making them invalid for new data to come in];

Divivier discloses all the steps shown above. Divivier does not disclose that prefetch buffer stores information regarding the size of the data in prefetch buffer. However Adler clearly discloses that depending on how many instructions are issued, reducing the size data in said prefetch buffer [col. 6, lines 8-25]; and depending on how many instructions are issued, reducing the data [count] for the number of instructions stored in said prefetch buffer, respectively [col. 6, lines 8-25]. Both Divivier and Adler are interested in buffering the data in most efficient way in a variable width instruction set architecture, also interested in keeping buffers as full as possible during each cycle. Adler teaches that by providing the indicators, such as SIZE, will allow the buffer to maintain the current state of the buffer and allow controller to fetch proper amount of data in the next cycle and make these decisions locally [col. 2, lines 42-51; Adler]. One of ordinary skill in the art at the time invention would have realized that by providing a size indicator to the system of Divivier would be advantageous because it would have kept prefetch buffer as full as possible. It would have been obvious to one of ordinary skill in the art to have provided Adler's size indicator to the system of Divivier, because

it would have provided a method for maintaining the prefetch buffer as full as possible during each cycle [col. 2, lines 1-9; Divivier] by knowing how full the buffer is and sending proper signal to fetch extra data.
NOTE: Adler discloses that table 150 with all indicators is in the controller. However Adler also discloses that the same table 150 could be part of the buffer itself [col. 6, lines 23-25]. One of ordinary skill in the art would have been able to put the indicators with the buffer as taught by Adler, because it would have provided the parameters in easy reach of the buffer itself thus saving time to access the data.

7. As to claim 2:

Divivier does not specifically discloses that when the number of stored instructions is less than the number of requested instructions, requesting a further instruction stream from said memory unit and combining the necessary instructions from said further instruction stream with the prefetched instructions. However Divivier clearly discloses that his invention is directed towards keeping buffer as full as possible during each cycle [col. 2, lines 1-9; Divivier]. It would have been obvious to one of ordinary skill in the art to have requested further instructions from memory and combined them with instructions in prefetch buffer because that would have kept prefetch buffer full for more efficient operation form the teaching of Divivier.

8. As to claim 3, Divivier discloses:

Method for providing a plurality of aligned instructions from an instruction stream provided by a memory unit for execution within a pipelined microprocessor comprising a first [fig. 1, unit 12] and second prefetch buffer [fig. 1, unit 14], whereby said prefetch buffers store prefetched instructions and additional information about the validity [fig. 3, units pf1 and pf0] of said prefetch buffers, said method comprising the steps of:

- in case both of said prefetch buffers contain invalid data [col. 8, lines 15-16]:

a) requesting an instruction stream and storing said instruction stream in said prefetch buffer [col. 7, lines 36-44]; [note: zero indicates invalid data, and if invalid data

is found; valid data is requested from external memory and stored in the prefetch buffer];

b) setting said data for validity in said prefetch buffer [col. 7, line 59 to col. 8, line 16];

c) issuing a requested number of instructions from said requested instruction stream [col. 7, line 59 to col. 8, line 16];

d) depending on how many instructions are issued, reducing the size data in said prefetch buffer, respectively [col. 8, line 57 to col. 9, line 44]; and

e) invalidating said validity data if all instructions from said prefetch buffer have been issued [col. 9, lines 24-35]; [NOTE: when buffer is empty all data positions are empty and now valid bits are set to "0" i.e. making them invalid for new data to come in]; also

- in case said prefetch buffer contains valid data [col. 8, lines 15-16]:

f) issuing a requested number of instructions from said prefetch buffer [col. 7, line 59 to col. 8, line 16];

g) depending on how many instructions are issued, reducing the data for the number of instructions stored in said prefetch buffer, respectively [col. 8, line 57 to col. 9, line 44]; and

h) invalidating said validity data if all instructions from said prefetch buffer have been issued [col. 9, lines 24-35]; [NOTE: when buffer is empty all data positions are empty and now valid bits are set to "0" i.e. making them invalid for new data to come in];

Divivier discloses all the steps shown above. Divivier does not disclose that prefetch buffer stores information regarding the size of the data in prefetch buffer. However Adler clearly discloses that depending on how many instructions are issued, reducing the size data in said prefetch buffer [col. 6, lines 8-25]; and depending on how many instructions are issued, reducing the data [count] for the number of instructions stored in said prefetch buffer, respectively [col. 6, lines 8-25]. Both Divivier and Adler are interested in buffering the data in most efficient way in a variable width instruction

set architecture, also interested in keeping buffers as full as possible during each cycle. Adler teaches that by providing the indicators, such as SIZE, will allow the buffer to maintain the current state of the buffer and allow controller to fetch proper amount of data in the next cycle and make these decisions locally [col. 2, lines 42-51; Adler]. One of ordinary skill in the art at the time invention would have realized that by providing a size indicator to the system of Divivier would be advantageous because it would have kept prefetch buffer as full as possible. It would have been obvious to one of ordinary skill in the art to have provided Adler's size indicator to the system of Divivier, because it would have provided a method for maintaining the prefetch buffer as full as possible during each cycle [col. 2, lines 1-9; Divivier] by knowing how full the buffer is and sending proper signal to fetch extra data.
NOTE: Adler discloses that table 150 with all indicators is in the controller. However Adler also discloses that the same table 150 could be part of the buffer itself [col. 6, lines 23-25]. One of ordinary skill in the art would have been able to put the indicators with the buffer as taught by Adler, because it would have provided the parameters in easy reach of the buffer itself thus saving time to access the data.

9. As to claim 4, Divivier discloses:

the number of stored instructions is less than the number of requested instructions, combining the necessary instructions from said other prefetch buffer with the prefetched instructions from said one prefetch buffer [col. 5, lines 58-67].

10. As to claim 5, Divivier discloses:

requesting an instruction stream and storing said instruction stream in the respective other prefetch buffer; and

setting said data for validity in said other prefetch buffer [col. 5, line 58 to col. 6, line 13];

11. As to claim 6:

Divivier does not disclose that additional information is set indicating which prefetch buffer contains older instructions. However Adler clearly discloses; information about which data is older in the buffer, by indicating which inbound data is being generated which is inbound data is waiting to be transmitted and which data still needs to be processed, this way Adler clearly indicates the age of the data [col. 6, lines 8-25]. Both Divivier and Adler are interested in buffering the data in most efficient way in a variable width instruction set architecture, and in keeping buffer as full as possible during each cycle. Adler teaches that by providing the indicators, such as age, will allow the buffer to maintain the current state of the buffer and allow controller to fetch proper amount of data in the next cycle to replace old data [col. 2, lines 42-51; Adler]. One of ordinary skill in the art at the time invention would have realized that by providing an age indicator to the system of Divivier would be advantageous because it would have kept prefetch buffer as full as possible. It would have been obvious to one of ordinary skill in the art to have provided Adler's age indicator to the system of Divivier, because it would have provided a method for maintaining the prefetch buffer as full as possible during each cycle [col. 2, lines 1-9; Divivier] by knowing which data is old and sending proper signal to fetch new data.

12. As to claim 7, Divivier discloses:

in case of one prefetch buffer containing invalid data the step of requesting an instruction stream and storing said instruction stream in the respective other prefetch buffer [col. 5, lines 35-52].

13. As to claim 8, Divivier discloses:

the step of requesting an instruction stream and storing said instruction stream in the respective other prefetch buffer [col. 5, line 58 to col. 6, line 13].

14. Claims 9-13 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Grochowski US. Patent 5,581,718, (hereafter Grochowski) in view of Adler et al., US. patent 4,811,284 (hereafter Adler).

As to claim 9, Grochowski discloses invention as claimed including a first prefetch buffer and first and second plurality of multiplexers [see figs. 1-3G] comprising the steps of:

- a first prefetch buffer [fig. 2, unit 23] coupled with said memory unit [fig. 2, unit 22]; whereby said first prefetch buffer stores prefetched instructions [col. 5, lines 45-55 and col. 6, lines 46-55],

- a first plurality of multiplexers [fig. 2, units 26] with input coupled with said first prefetch buffer [and second prefetch buffer] for selecting a certain number of instructions and with outputs [col. 3, lines 6-39],

- a second plurality of multiplexers [fig. 2, unit 27], with inputs coupled with said outputs of said first multiplexers for aligning [col. 5, lines 52-57] said selected instructions [col. 5, lines 45-67];

Grochowski discloses all the apparatus shown above including first plurality of multiplexers with inputs connected to first prefetch buffer and second prefetch buffer. Grochowski does not disclose that the first plurality of multiplexers has inputs connected to the first prefetch buffer and memory. However such limitations are merely a matter of design choice and would have been obvious in the system of Grochowski. Grochowski teaches alignment of instructions with two large buffers supplying these instructions. The limitations in claim 9 do not define a patentable distinct invention over that in Grochowski since both the invention as a whole and Grochowski are directed to aligning the instructions from storage area. The amount of instructions taken from different storage area for the invention as a whole presents no new or unexpected results, so long as the instructions are successfully aligned. Therefore, to have instructions also taken form memory instead of buffer would have been a matter of obvious choice to one of ordinary skill in the art.

Grochowski discloses all the apparatus shown above. Grochowski does not disclose that prefetch buffer also stores information regarding the size or validity of the data in prefetch buffer. However Adler clearly discloses; a SIZE indicator and validity indicator [by indicating which data is being generated, which is waiting to be transmitted and which data still needs to be processed, Adler indicates the validity of the data] [col. 6, lines 8-25]. Both Grochowski and Adler are interested in buffering the data in most efficient way. Adler teaches that by providing the indicators, such as SIZE and validity will allow the buffer to maintain the current state of the buffer locally and allow controller to fetch proper amount of data in the next cycle and make these decisions locally [col. 2, lines 42-51; Adler]. One of ordinary skill in the art at the time invention would have realized that by providing a size indicator to the system of Grochowski would be advantageous because it would have allowed the data transfer decision be made locally. It would have been obvious to one of ordinary skill in the art to have provided Adler's size and validity indicator to the system of Grochowski, because it would have provided a mechanism to make decisions locally regarding size of the data to be transferred, and marking valid data in buffer.
NOTE: Adler discloses that table 150 with all indicators is in the controller. However Adler also discloses that the same table 150 could be part of the buffer itself [col. 6, lines 23-25]. One of ordinary skill in the art would have been able to put the indicators with the buffer as taught by Adler, because it would have provided the parameters in easy reach of the buffer itself thus saving time to access the data.

15. As to claim 10, Grochowski discloses:

at least a second prefetch buffer [fig. 2, unit 24] coupled with said memory unit and with inputs of said first multiplexers is provided [col. 5, lines 45-67].

16. As to claim 11, Grochowski discloses:

Grochowski discloses two buffers with different instructions. Grochowski does not disclose that prefetch buffers store information regarding the age of the data.

However Adler clearly discloses; information about which data is older in the buffer. By indicating which inbound data is being generated which is inbound data is waiting to be transmitted and which data still needs to be processed, Adler clearly indicates the age of the data [col. 6, lines 8-25]. Both Grochowski and Adler are interested in buffering the data in most efficient way. Adler teaches that by providing the indicators, such as age of the data will allow the buffer to maintain the current state of the buffer locally and allow controller to fetch proper amount of data in the next cycle and make these decisions locally [col. 2, lines 42-51; Adler]. One of ordinary skill in the art at the time invention would have realized that by providing an age indicator to the system of Grochowski would be advantageous because it would have allowed the data transfer decision be made locally and allowed newer data be loaded in the buffers earlier. It would have been obvious to one of ordinary skill in the art to have provided Adler's age indicator to the system of Grochowski, because it would have provided a mechanism to allowed the data transfer decision be made locally and allowed newer data be loaded in the buffers earlier.

NOTE: Adler discloses that table 150 with all indicators is in the controller. However Adler also discloses that the same table 150 could be part of the buffer itself [col. 6, lines 23-25]. One of ordinary skill in the art would have been able to put the indicators with the buffer as taught by Adler, because it would have provided the parameters in easy reach of the buffer itself thus saving time to access the data.

17. As to claim 12, Adler discloses:

a prefetch buffer control unit [fig. 5, unit 8] for selecting and read/write control of said first and second prefetch buffers and for updating said additional information in said first and second prefetch buffers [col. 5, lines 7-23].

18. As to claim 13, Grochowski discloses:

each instruction stream provided by said memory unit comprises at least four words containing a plurality of instructions, each prefetch buffer stores at least four

words containing a plurality of instructions, and wherein the first multiplexers consist of at least four multiplexers [fig. 2, unit 25, total eight multiplexers] having inputs and an output, respectively for selecting one of said words from one of said instruction stream or prefetch buffers, and wherein the second multiplexers consist of at least four multiplexers [fig.2, unit 27] having inputs and an output, respectively, for aligning said selected words from said first multiplexers [col. 3, lines 6-39];

Regarding claims 13, although Grochowski does not specifically disclose the number of inputs [three and four] that are going into the first or second multiplexers, such limitations are merely a matter of design choice and would have been obvious in the system of Grochowski. Grochowski teaches that his multiplexer has two inputs because there are two registers from which the data is being selected. The limitations in claim 13 do not define a patentable distinct invention over that in Grochowski since both the invention as a whole and Grochowski are directed to aligning the instructions. The number of inputs to multiplexers are inconsequential for the invention as a whole and presents no new or unexpected results, so long as these instructions are aligned Therefore, to provide different inputs to the multiplexers would have been a matter of obvious choice to one of ordinary skill in the art.

Other prior art cited

19. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.
    a. Cai et al. (US. patent 5,909,566) "Microprocessor circuits, systems and methods for speculatively executing instruction using its most recently used data while concurrently prefetching data for the instruction".
    b. Narayan et al. (US. patent 6,202,142) "Microcode scan unit fro scanning microcode instructions using predecode data".

c. Watkins (US. patent 5,854,911) "Data buffer prefetch apparatus and method".

d. Tran (US. patent 6,122,729) "Prefetch buffer which stores a pointer indicating an initial predecode position".

e. McMahan (US. patent 5,835,967) "Adjusting prefetch size based on source of prefetch address".

Contact information

20. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gautam R. Patel whose telephone number is (703) 308-7940. The examiner can normally be reached on Monday through Thursday from 7:30 to 6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Eddie P. Chan, can be reached on (703) 305-9712. The fax phone number for this Group is (703) 306-5404.

Any inquiry of a general nature or relating to the status of this application should be directed to the group receptionist whose telephone number is (703) 305-3900.

GRP

Gautam R. Patel
Patent Examiner
Group Art Unit 2183

May 12, 2001

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